COURSE PROSPECTUS

Name of the Division: *Smart Technology & Education Division (STED)*

Name of the Course: *PG Program in VLSI SoC Design and Verification*

Course Code: *VS500*

Mode of Conduction: *Online*

Starting Date: *06-11-2023*

Duration: *600 Hours /26 Credits*

Course Fee: ***₹ 40,000/- Including Taxes***

Course Coordinator: *Nandakumar R /Sreejeesh SG Ph.: 9995427802/9447769756*

Preamble:

The complex Very Large Scale Integrated (VLSI) systems are built on System on Chips (SoCs). In a SoC usually, many processor cores and the essential peripherals are wrapped. To design a SoC, knowledge in processor architectures, various bus protocols, etc. are essential. Also, the SoC verification is more challenging as it involves the verification of many complex scenarios. Therefore usually the SoCs are emulated on a Field Programmable Gate Array (FPGA) and the real chip verification will be carried out before spin. This VLSI SoC Design and Verification course focuses on building the necessary industry skills required to work in SoC Design/Verification/FPGA Emulation projects. The course focuses on industry-standard Advanced RISC Machine (ARM) processors based SoC design, verification, and FPGA emulation. The necessary skills (Verilog HDL Coding for synthesis, FPGA Architecture and Programming, System Verilog based Verification, etc.) required to perform industry jobs are covered in this course. The course will transform the successful participants into industry-ready employable engineers. In addition, it helps to conceive and hand-hold startup industries in the VLSI SoC Design/Verification/Emulation domain.

Objective of the Course:

PG Program in VLSI SoC Design and Verification Course is intended to impart skills essential for VLSI Circuits design, ARM based SoC design, Verification, Software programming.

Outcome of the Course:

The successful participants will have;

1. In-depth knowledge, skills and comprehensive understanding about the Electronics fundamentals, SoC Design and Verification methodologies and industry practices followed by VLSI Design Companies across the world.
2. Ready employability in multiple roles available in VLSI Industry.
3. Refined skillsets, knowhow and confidence needed for entrepreneurship in VLSI Design and Verification industry.

Expected Job Roles:

- *RTL Design Engineer.*
- *RTL Verification Engineer.*
- *VLSI/SoC Design & Verification Engineer.*
- *Front-end ASIC Design & Verification Professional.*
- *FPGA Design Engineer.*
- *SoC Emulation /Validation Engineer.*
- *Embedded Software Engineer.*
- *Embedded Hardware Engineer.*

Course Structure: The VS500 course has seven modules including project work. The Participants are required to do a project work in any one of the modular areas, to be eligible for issue of PG Certificate.

The modules are as follows:

Module Code*	Module Name	Duration (Hrs)			Credit
		Total	Theory	Lab	
VS 501	Embedded C and ARM Cortex Microcontrollers	65	13	52	3 (1+2)
VS 502	VLSI Fundamentals	65	13	52	3 (1+2)
VS 503	FPGA Architecture and Programming using Verilog HDL	65	13	52	3 (1+2)
VS 504	ARM based SoC Design	65	13	52	3 (1+2)
VS 505	Advanced ARM SoC Design	65	13	52	3 (1+2)
VS 506	SoC Verification	65	13	52	3 (1+2)
VS 507	Project	210		210	8
	Total	**600**	**78**	**522**	**26**

**These modules are conducted as workshops. Modular admission is available and prerequisites for the modular admission are applicable, only to the B.Tech ongoing students. Those who are completing all the modules are eligible for PG Certificate on Submission of Original/ Provisional Certificate of Qualifying Degree.*

Other Contents

I. **Course Fees**: Course fee is ₹40,000/- (All taxes are included)

* *Taxes Included (Currently GST @18%), and revisions, if any by Government shall be applicable at the time of payment.*

** *B.E/B.Tech Ongoing Students should submit a bonafide certificate from HoD of the respective college of study and should meet prerequisite as mentioned in the syllabus.*

II. **Registration Fee:** An amount of ₹1000/- (including all taxes as applicable) (will be adjusted to the total fee payable) should be paid at the time of registering for the course.

This fee shall be considered as part of course fee, if the student joins the course. If a student register and pay for more than one course and join for any one course, all such amount will be adjusted against the course fee payable. If the candidate does not join or fails to complete the course the amount will be forfeited.

However above the registration fee shall be refunded on few special cases as given below.

- Course postponed and new date is not convenient for the student
- Course cancelled in advance, well before the admission date

III. **Course Fee Installment Structure**:

Students can pay the full fees of (₹40,000/-) in advance or as installments as given below.

Fees	***Amount**	**# Due Date (on or before)**
Registration Fee	₹*1000/-*	During Online Registration
1st Installment	₹ *20,000/-*	***06.11.2023***
2nd Installment	₹ *19,000/-*	***30.01.2024***
Total Fee	₹ 40,000/-	***30.01.2024***

*Taxes Included (Currently GST @18%), and revisions, if any by Government shall be applicable at the time of payment.

Fine will be applicable to late fee payment as given below;

Sl. No.	Description	Fine
1.	Late fee payment within two weeks after due date	18% (annually) of the outstanding dues
2.	After second week of due date the candidate has to pay readmission fees along with the fine	Readmission fee ₹250/- plus fine of 18% (annually) of the outstanding dues
3.	The candidate has to discontinue the course after third week from the due date	

IV. **Eligibility:** B.E /B.Tech completed students of the following branches:

Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Biomedical /Computer Science/Information Technology.

B.E /B.Tech ongoing students of the above branches are eligible to enroll for the modular workshop subject to meeting the pre-requisite for each module as mentioned in *syllabus*.

For more details about the policy refer:
http://nielit.gov.in/sites/default/files/course/NIELITCalicutPoliciesShortTermCourses.pdf

V. **Number of Seats :***40*

VI. **Selection of candidates:** Selection is based on the marks in the qualifying Degree.

VII. **Test/Interview:** *Not Applicable*

VIII. **Counseling/Admission** : *06-November-2023*

IX. **Important Dates:**

***Last date** for receiving online application for the course with payment of ₹1000/- for registration. Candidates applying after this date will be considered in spot admission against vacancy.*	***01.11.2023***
*Publication of **First selection list** in our Website.*	***03.11.2023***
*Last date for Payment of the **first installment fee of ₹20,000/-.***	***06.11.2023***
Counseling and Admission	***06.11.2023***
Commencement of Classes	***06.11.2023***

X. **Course Timings**: Classes will be *between 9.30 am to 5.00 pm. **The hands-on session using Hardware Lab at NIELIT Calicut**.*

XI. **Placement** : *visit http://nielit.gov.in/content/placement-3*

XII. **Lab Facilities :** http://nielit.gov.in/calicut/calicut/content/vlsi-design-group

XIII. **Course Contents :** Course Syllabus

Click here for General Terms and Conditions – Applicable to all courses